

# A proposal to include fabrication documentation in Gerber

**Rev 2017.10**

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**Draft for review only**

**Please send your comments to [gerber@ucamco.com](mailto:gerber@ucamco.com)**

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# 1 Preface

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Since decades, Gerber is the standard for describing the 2D images – copper layers, solder mask, drills – in PCB fabrication data. Attributes added with Gerber X2 provide a standard to 'add intelligence to the image' by defining the layer structure – which file is which layer – identify via and SMDs component, pin numbers and reference descriptions.

But PCB fabrication data is not just about images. It includes PCB characteristics such as finish, overall thickness, materials and the assembly array definition. They are essential for the quoting, planning, engineering, CAM and fabrication of the bare board as well as for determining the optimal assembly array.

Today there is no standard governing this data. It is transferred informally in drawings and texts and handled manually, wasting time and risking errors. This is a glaring hole in the current workflow.

The industry goal is to process the PCB fabrication data automatically, at least for standard boards. This document is a draft for an evolutionary extension of the Gerber format with a standard for conveying PCB characteristics. It is a discussion document to solicit input from the Gerber user community and reach a consensus. The proposal will go through several revisions based on this input.

Please send your comments to [gerber@ucamco.com](mailto:gerber@ucamco.com)

## 2 Design considerations

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PCB layout software typically focus on the image data and rarely 'knows' product parameters such finishes and colors – it does not need to. Consequently, such parameters will be defined by other applications, typically far simpler than a full-blown CAD system. An application to define the IPC class or a legend color cannot reasonably be expected to handle Gerber images. The product parameters must therefore be stored in a separate, dedicated file, apart from the images. Let us call this file the Gerber job file because it pertains to the whole job, not to a single layer.

These parameters are not tied to a layer or a graphics object but to the PCB as a whole. Thus they cannot be conveyed effectively by X2 attributes. The X2 attributes are tied to the image and must be set by graphically sophisticated layout software.

The standard must be easy to adopt and to implement. Partial implementations must be easy as some applications may only 'know' a few PCB characteristics. Better partial information than no information. . Simple PCBs must be specified in a simple manner.

We maintain the Gerber's hallmark of simplicity and human-readability.

The new standard must be compatible with existing workflows: legacy software that cannot handle the new standardized parameters must continue to function, in the old manual way, and new software that does read them must handle legacy data sets without them.

The draft intentionally defines the technical PCB parameters only, *not* commercial conditions such as delivery times and address, pricing, quantities. We need a standard definition of the PCB as it is. The same PCB can be ordered at different times, with different commercial conditions. The PCB definition must remain untouched when the same PCB is ordered at another time, from another company, in other quantities.

We intentionally do *not* specify default values. The first reason is that partial implementations must be possible or adding parameters in subsequent steps. If the format has defaults one cannot know whether an absent parameter is not yet defined or that the default value is intended; without defaults it is clear: a missing parameter is not yet defined . The second reason is that a mere data transfer format must not pretend to specify what default parameters the PCB industry should use. E.g. it is surely not up to the Gerber format to decree what the copper thicknesses would be. The format must allow to describe the PCB perfectly but not legislate what the normal and what the exceptional value of a PCB parameter is.

The draft intentionally does *not* cover assembly arrays. As they are not single PCBs their definition lies *outside* the scope of this specification. Layout systems are generally designed to generate a single PCB rather than arrays. This makes sense: assembly panels are typically not decided by the designer but by the assembler. The assembly panel is a separate entity and we feel it should be defined in a separate structure referring to a single PCB. After all, the same PCB may be assembled in different panels at different times, or a panel may contain multiple PCB's. What we can do is to make the assembler's life easier by making the data that he needs to define the assembly array – the XY size of the PCB - is easily found, and can be extracted without processing fully-fledged Gerber image files.

The draft intentionally does *not* cover the full material stackup definition. For the majority of PCBs there is no need to specify the full stackup: it is sufficient to specify overall thickness and outer and inner copper thicknesses. For simplicity's sake we now define just these parameters. In due course we will extend the Gerber job specification to handle the material stackup.

However, a full stackup for flex-rigid, special materials, impedance control can be quite complex. The challenge will be to define it in such a way that that simple things remain simple, but complex structures can also defined unequivocally.

This draft intentionally *only* covers the parameters for standard PCBs. The aim is to get going as quickly as possible and then simplicity and restraint is a plus. Parameters for more complex PCBs can be added later, as the needs develops. One may think the need for standardization is greater for complex boards but this is not so. Complex boards have a margin that allows manual data entry and communication between designer and fabricator. For simple boards the data must be automated as there is simply no margin for discussions and a lot of manual work.

# 3 Draft Specification

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## 3.1 Job Attributes

Job attributes provide information about the entire PCB, not linked to a specific layer.

Job attributes are set using the TJ command. They follow the syntax of the other attributes.

**<TJ command> = %TJ<AttributeName>[,<AttributeValue>]\*%**

**<AttributeValue> = <Field>{,<Field>}**

The attribute name must follow the syntax in section 3.6.5, fields the one in 3.6.6. The name is unique and cannot be used for any other attribute, even of another type. Once an attribute is defined, it cannot be redefined.



### Example:

```
%TJ.B_Size_X,160*%
```

This states the board size in X is 160 units.

## 3.2 New File Function: Job file

The single PCB job attributes are concentrated in a separate file, the Gerber job file. One job file per PCB. The job file is identified with the new file function `JobFile`. This indicates the file does not describe a single layer or entity in the PCB job, but characteristics pertaining to the job as a whole, such as the finish or overall thickness. The Gerber job file can only contain job attributes, not image data. Applications do not need to be image-savvy to process it.

Example:

```
%TF.FileFunction,JobFile*%
```

To find the job file easily in a fabrication data archive it has its own file extension “.gbrjob”. An example job file name is

```
Controller54382rev4.gbrjob
```

Although the job file is still a Gerber file another file extension is warranted as it will often be other applications that process it than the ones that process the images.

### 3.3 Single PCB job attributes

<n> = integer

<d> = decimal

<s> = string

<color> = (Red|Green|Blue|White|Black|R<n>G<n>B<n>) (<n> is an integer from 0 to 255)

<presence> = (None|TopOnly|BotOnly|Both)

Attribute name + values	Usage,
<b>Overall Board Parameters</b>	
.B_Owner, <s>	Reference of the design owner, as used by himself
.B_ID, <s>	Board id or reference as used by the design owner/
.B_Size_X, <d>	Board size, being the size of the axis-aligned enclosing rectangle of the board outline and its tolerances.  Positive decimals in the unit of the MO command
.B_Size_Y, <d>	
.B_Size_Tol+, <d>	
.B_Size_Tol-, <d>	
.B_LayerNum, <n>	Number of copper layers.
.B_Overall_Thickness, <d>	Overall board thickness and its tolerances. Positive decimals in the unit of the MO command.  "Over" stands for measured <i>over</i> e.g. mask, substrate etc.
.B_Overall_Thickness_Tol+, <d>	
.B_Overall_Thickness_Tol-, <d>	
.B_Overall_Thickness_Over, <d>	
.B_Copper_Thickness_Out, <d>	Final copper thicknesses. Positive decimals in the unit of the MO command.  Thickness_Holes is the plating thickness.
.B_Copper_Thickness_Inr, <d>	
.B_Copper_Thickness_Holes, <d>	
.B_SolderMask_Present, <presence>	This attribute defines whether the layer must be present in the <i>physical bare</i> PCB. (This is not the same as the presence of the Gerber file – a legend Gerber file may be present but one may not want a legend in this particular fabrication run.) As paste is not part of the bare PCB there is no corresponding attribute.
.B_Legend_Present, <presence>	
.B_PeelableMask_Present, <presence>	
.B_Carbon_Present, <presence>	
.B_SolderMask_Color, <color>	Can be overruled by the values in the stackup details.
.B_Legend_Color, <color>	

<code>.B_Substrate, &lt;substrate&gt;{, &lt;substrate&gt;}</code> with <code>&lt;substrates&gt;= (FR4 Polyimide Polyolefin Al PTFE Teflon Ceramic &lt;s&gt;)</code>	The substrate(s) used in the PCB.
<code>.B_IPC-600-Class, (1 2 3 NA)</code>	
<code>.B_Standard, &lt;s&gt;</code>	MIL, JSS, IPC6012B, PCA600,... We need formal pre-defined strings and a free string for other cases. TBD.
<code>.B_IPC-2221-Type, (1 2 3 4 5 6 &lt;s&gt;)</code>	The board type according to IPC-2221. There are six primary board types: <ul style="list-style-type: none"> <li>• Type 1 - Single-sided</li> <li>• Type 2 - Double-sided</li> <li>• Type 3 – Multilayer, TH components only</li> <li>• Type 4 – Multilayer, with TH, blind and/or buried vias</li> <li>• Type 5 - Multilayer metal-core board , TH components only</li> <li>• Type 6 - Multilayer metal-core</li> </ul>
<code>.B_Foil, (Electro-Deposited Rolled &lt;s&gt;)</code>	Copper foil type
<code>.B_Finish, (HASL Immersion (tin nickel silver gold) Enig Epenig OSP HT_OSP None &lt;s&gt;)</code>	
<code>.B_ViaFilling, (Yes no)</code>	This attribute indicates whether filled via's are present. Yes does not mean all are filled. Which ones they are is determined by .AperFunction in the Gerber drill files.
<code>.B_Logo, (Yes No)</code>	
<code>.B_RoHS, (Yes No)</code>	
<code>.B_UL, (Yes No)</code>	
<code>.B_ITAR, (Yes No)</code>	
<code>.B_EdgePlating, (Yes No)</code>	
<code>.B_ImpedanceControlled, (Yes No)</code>	
<code>.B_HardGold, (Yes No)</code>	
<code>.B_EdgeConnector, (Yes No)</code>	
<code>.B_EdgeConnectorBevelled, (Yes No)</code>	
<code>.B_Notes, &lt;s&gt;</code>	A free string with informal information.

### Intended design rules

The main design rules used to create the layout. These parameters may seem superfluous as these values are reflected in the image. However, it is convenient to know these values without analyzing the Gerber image files and knowing the design intent is useful in CAM when there are problems.

<code>.D_PadToPad_(Inr Out),&lt;d&gt;</code>	
<code>.D_PadToTrack_(Inr Out),&lt;d&gt;</code>	
<code>.D_PadToRegion_(Inr Out,&lt;d&gt;)</code>	Regions are here used to represent copper pours.
<code>.D_TrackToTrack_(Inr Out),&lt;d&gt;</code>	
<code>.D_TrackToRegion_(Inr Out),&lt;d&gt;</code>	
<code>.D_RegionToRegion_(Inr Out),&lt;d&gt;</code>	
<code>.D_MinLineWidth_(Inr Out),&lt;d&gt;</code>	
<code>.D_MinRing_(Inr Out),&lt;d&gt;</code>	
<code>.D_MinHoleSize,&lt;d&gt;</code>	
<code>.D_MinClearanceToProfile,&lt;d&gt;</code>	
<code>.D_Notes,&lt;s&gt;</code>	A free string with informal information.



## Materials Stackup

The material stackup attributes are constructed with the two following items.

The first defines the layer type:

**<LayTyp> = Legend|SolderMask|Copper|Dielectric|PeelableMask|Coverlay|Bondply|Adhesive|Other <s>)**

The second defines the layer index|

**<LayIdx> =L<d>**

The layer index is constructed around the copper layer number. The integer refers to a copper layer, with L2.0 being copper layer 2. The decimal fraction refers to a position below that copper layer. L2.1 is the first layer below copper layer 2, normally the dielectric. L0.1 is above copper layer 1, e.g the top solder mask.

Layer indexes must occur in the file in the same order as in the physical stackup, starting with the top side, which has the lowest index. If any .S attribute is defined the layer type of *all* layers must be defined; in other words no layers can be skipped in the sequence of indices.

For flex-rigid boards the one can define a number of substacks, identified by an index, of the master stack

.S_<LayIdx>_Type,<LayTyp>	Layer Type
.S_<LayIdx>_Thickness,<d>	Thickness in MO units
.S_<LayIdx>_Color,<color>	
.S_<LayIdx>_Note,<s>	A note on the layer or material.
.S_<LayIdx>_DConstant,<d>	Dielectric constant.
.S_<LayIdx>_LossTangent,<d>	Loss Tangent.
.S_<LayIdx>_Conductivity,<d>	Conductivity in S/m.
.S_Substack_<n>,{LayIdx}	A substack as occurring in flex-rigid boards. The layer indexes must be in consecutive order. <n> is a substack index for reference.
.S_Notes,<s>	A free string. Notes on the stackup in general.

An example of a four layer board, with solder mask on both sides and legend on top:

```
G04*
G04 Material Stackup*
G04*
%TJ.S_L0.1_Type,Legend*%
%TJ.S_L0.1_Color,White*%
G04*
%TJ.S_L0.2_Type,SolderMask*%
%TJ.S_L0.2_Color,Green*%
%TJ.S_L0.2_Thickness,0.02500*%
G04*
%TJ.S_L1.0_Type,Copper*%
%TJ.S_L1.0_Thickness,0.03556*%
G04*
%TJ.S_L1.5_Type,Dielectric*%
%TJ.S_L1.5_Thickness,1.483*%
G04*
%TJ.S_L2.0_Type,Copper*%
%TJ.S_L2.0_Thickness,0.01500*%
G04*
%TJ.S_L2.5_Type,Dielectric*%
%TJ.S_L2.5_Thickness,1.483*%
G04*
%TJ.S_L3.0_Type,Copper*%
%TJ.S_L3.0_Thickness,0.01500*%
G04*
%TJ.S_L3.5_Type,Dielectric*%
%TJ.S_L3.5_Thickness,1.483*%
G04*
%TJ.S_L4.0_Type,Copper*%
%TJ.S_L4.0_Thickness,0.03556*%
G04*
%TJ.S_L4.1_SolderMask*%
%TJ.S_L4.1_Thickness,0.02500*%
%TJ.S_L4.1_Color,Green*%
```

## Layer Structure

These attributes define function and polarity of each image file in the layer structure.

Note that the file attributes .FileFunction and .FilePolarity in each file in the layer structure. Having this information available in the job file has the benefit that it is available without parsing each Gerber image file. It makes it easier for an application to load the files it needs. The redundancy adds to the robustness.

This range of attributes has a name with the following structure.

.L\_ "<file function>"(Positive|Negative),<Path>

The <file function> part of the attribute name can take any value of the .FileFunction file attribute.

<Path> is a string with the path to the corresponding Gerber file.

For example:

```
%TJ.L_ "Copper, L1, Top", Positive, AZ2375EM_Top_Copper.gbr*%
```

There are no default values. If a parameter is not present it is not defined in Gerber. The parameter is then defined otherwise; typically reasonably fabricator defaults are used.

Of course CAD systems 'know' board size and layer count, both of which are required to define assembly panels. Ideally, CAD systems will output a simple job file with board size and layer count (and other parameters they might know), allowing assemblers to define their panels automatically, without having to process Gerber image files.

## 3.4 Minimal CAD Job File

Below is the minimal job file that CAD must include in the fabrication data. It contains board size and layer count, and ideally any other parameters the CAD software 'knows'. The board size is the essential information needed to define the assembly panel. Other applications can read and extend this initial job file with more information.

```
G04 Mininal CAD Gerber job file*
%TF.FileFunction,JobInfo*%
%TF.Part,SinglePCB*%
%MOMM*%
%TJ.B_Size_X,160*%
%TJ.B_Size_Y,50.8*%
%TJ.B_LayerNum,6*%
M02*
```

## 3.5 Example: Basic Job File

This example contains the main overall board parameters.

```
G04 Gerber job file with the basic overall board parameters*
%TF.FileFunction,JobInfo*%
%TF.Part,SinglePCB*%
%TF.GenerationSoftware,Ucamco,UcamX,2016.12*%
%TF.CreationDate,2017-01-02T16:58:41+01:00*%
%TF.ProjectId,Sample file,6B69742D6465762D636F6C64666697265,1*%
%MOMM*%
G04 Single PCB fabrication instructions*
%TJ.B_ID,AZ2375EM*%
%TJ.B_Size_X,160*%
%TJ.B_Size_Y,50.8*%
%TJ.B_LayerNum,6*%
%TJ.B_Overall_Thickness,1.6*%
%TJ.B_Copper_Thickness_Out,0.035*%
%TJ.B_Copper_Thickness_Inr,0.012*%
%TJ.B_SolderMask_Present,Both*%
%TJ.B_Legend_Present,TopOnly*%
%TJ.B_ROHS,Yes*%
M02*
```

## 3.6 Example: More Complete Job File

This example also contains the material stackup and layer structure

```
G04 Gerber job file with some stackup info and the layer structure.*
%TF.FileFunction,JobInfo*%
%TF.Part,SinglePCB*%
%TF.GenerationSoftware,Ucamco,UcamX,2016.12*%
%TF.CreationDate,2017-02-20T20:58:41+01:00*%
%TF.ProjectId,Sample file,6B69742D6465762D636F6C6466697265,1*%
%MOMM*%
G04 Single PCB fabrication instructions*
G04*
G04 Overall board parameters*
G04 -----*
%TJ.B_Owner,Intergalactic Corporation*%
%TJ.B_ID,AZ2375EM*%
%TJ.B_Size_X,160*%
%TJ.B_Size_Y,50.8*%
%TJ.B_LayerNum,2*%
%TJ.B_SolderMask_Present,Both*%
%TJ.B_Legend_Present,TopOnly*%
%TJ.B_IPC-600-Class,2*%
%TJ.B_Finish,Immersion Gold*%
%TJ.B_Overall.Thickness,1.6*%
G04*
G04 Material Stackup*
G04 -----*
%TJ.S_L0.1_Type,Legend*%
%TJ.S_L0.1_Color,White*%
G04*
%TJ.S_L0.2_Type,SolderMask*%
%TJ.S_L0.2_Color,Green*%
%TJ.S_L0.2_Thickness,0.02500*%
G04*
%TJ.S_L1.0_Type,Copper*%
%TJ.S_L1.0_Thickness,0.03556*%
G04*
%TJ.S_L1.5_Type,Dielectric*%
%TJ.S_L1.5_Thickness,1.483*%
G04*
%TJ.S_L2.0_Type,Copper*%
%TJ.S_L2.0_Thickness,0.01500*%
G04*
%TJ.S_L2.5_Type,Dielectric*%
%TJ.S_L2.5_Thickness,1.483*%
G04*
%TJ.S_L3.0_Type,Copper*%
%TJ.S_L3.0_Thickness,0.01500*%
G04*
%TJ.S_L3.5_Type,Dielectric*%
```

```

%TJ.S_L3.5_Thickness,1.483*%
G04*
%TJ.S_L4.0_Type,Copper*%
%TJ.S_L4.0_Thickness,0.03556*%
G04*
%TJ.S_L4.1_SolderMask*%
%TJ.S_L4.1_Thickness,0.02500*%
%TJ.S_L4.1_Color,Green*%
G04*
G04 Layer Structure*
G04-----*
%TJ.L_ "Paste,Top",Positive,AZ2375EM_Top_SMT_Paste.gbr*%
%TJ.L_ "Legend,Top",Positive,AZ2375EM_Top_Silk.gbr*%
%TJ.L_ "SolderMask,Top",Negative,AZ2375EM_Top_Solder.gbr*%
%TJ.L_ "Copper,L1,Top",Positive,AZ2375EM_Top_Copper.gbr*%
%TJ.L_ "Copper,L2,Inr",Positive,AZ2375EM_Bot_Copper.gbr*%
%TJ.L_ "Copper,L3,Inr",Positive,AZ2375EM_Top_Copper.gbr*%
%TJ.L_ "Copper,L4,Bot",Positive,AZ2375EM_Bot_Copper.gbr*%
%TJ.L_ "SolderMask,Bot",Negative,AZ2375EM_Bot_Solder.gbr*%
%TJ.L_ "Plated,1,4,PTH",Positive,AZ2375EM_Drill_Plated.gbr*%
%TJ.L_ "NonPlated,1,4,NPTH",Positive,AZ2375EM_Drill_plated.gbr*%
%TJ.L_ "AssemblyDrawing,Top",Positive,AZ2375EM_Top_Assembly.gbr*%
M02*

```

# 4 Revisions

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## Rev 2017.10

New concept for material stackup, much simpler. Added support for flex and flex/rigid. We especially thank Richard Attrill who provided valuable input.

Replaced the separator “.” Within attribute names by an “\_” to avoid confusion with the decimal point and the point indicating a standard attribute.

## Rev 2017.09

Jean-Pierre Charras developed the first job file output and this triggered helpful comments.

Additions:

- .B.Type
- .B.Foil
- .D.MinClearanceToOutline
- .D.MinRing.(Inr|Out).
- Polarity to layer structure.
- Support for multiple laminates for RF boards as suggested by KiCad developers.

Changes:

- Replaced (Inner|Outer) by (Inr|Out) for consistency with file function.
- Changed the index of the dielectric from a pure number <n> to Dn for clarity.
- Improve values of .B.SolderMask.Present and other present attributes.
- Changed file extension to “.gbrjob”

## Rev 2017.08

Changed job file extension from “\_job.gbr” to “.gbj”

Formalize a number of parameter values. Split design rules in inner and outer.

## Rev 2017.03

Error corrections and improvements suggested by Paul Wells-Edwards, Remco Poelstra, Rik Breemeersch. Added parameters suggested by Ken Caluwaerts.

Made a more complete list of board parameters.

## Rev 2017.01

Initial version

parameters, added intended design rules, material stackup and layer structure definition.

# 5 Copyright

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