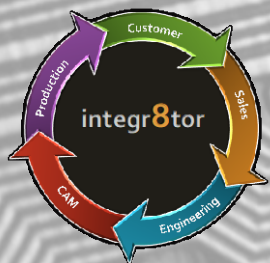






# Integr8tor v2020.12



版本概述

## 您的竞争优势...

- 背钻PCB的QED分析 
- Altium PCB 输入连接器 
- DPMX (IPC-2581) 数据输入 
- 基于铜权重的QED条件格式 
- 和更多!

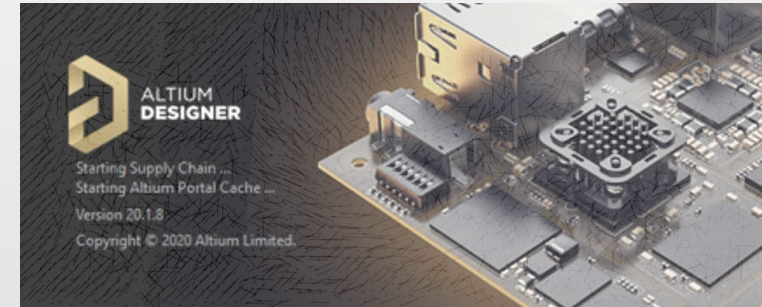
## 背钻PCB的QED分析

- 全自动输入背钻产品
- 全面的背钻特定QED分析  
(新选配功能)

INITIAL	FORMAT	RENAMED	FUNCTION
7770_Non_Switch_081015-bd-1-4.drl	excellon2	drl_1_4	backdrill
7770_Non_Switch_081015-bd-1-6.drl	excellon2	drl_1_6	backdrill
7770_Non_Switch_081015-bd-1-8.drl	excellon2	drl_1_8	backdrill
7770_Non_Switch_081015-bd-24-10.drl	excellon2	drl_10_24	backdrill
7770_Non_Switch_081015-bd-24-12.drl	excellon2	drl_12_24	backdrill
7770_Non_Switch_081015-bd-24-15.drl	excellon2	drl_15_24	backdrill
7770_Non_Switch_081015-bd-24-17.drl	excellon2	drl_17_24	backdrill
7770_Non_Switch_081015-bd-24-19.drl	excellon2	drl_19_24	backdrill
7770_Non_Switch_081015-bd-24-21.drl	excellon2	drl_21_24	backdrill
7770_Non_Switch_081015-bd-24-7.drl	excellon2	drl_7_24	backdrill
7770_Non_Switch_081015-bd-24-8.drl	excellon2	drl_8_24	backdrill

## Altium PCB 输入连结

- 集成了Altium Designer软件以完全自动输入Altium本机.pcbdoc文件
- 抢先成为报价!  
(新选配功能)



## DPMX (IPC-2581) 数据输入

- 完全自动接受新兴标准DPMX格式的数据
- 通过接受任何客户的首选格式来增加市场份额

(新选配功能)



## 根据铜的比重

- 当您将QED中的间隙和线宽度与铜权重的厚度相关时，QED PDF上的红色单元格会告诉您更多信息。

(QED PDF报告补充)

```
61 Example:
62 <FormattingRule id="minimumtrack">
63   <Condition>lessthan</Condition>
64   <Value1>0.075</Value1>
65   <ThicknessRule id="base">
66     <Condition>lessthan</Condition>
67     <Value1>0.035</Value1>
68   </ThicknessRule>
69 </FormattingRule>
70 <FormattingRule id="minimumtrack">
71   <Condition>lessthan</Condition>
72   <Value1>0.1</Value1>
73   <ThicknessRule id="base">
74     <Condition>between</Condition>
75     <Value1>0.035</Value1>
76     <Value2>0.070</Value1>
77   </ThicknessRule>
78 </FormattingRule>
79 <FormattingRule id="minimumtrack">
80   <Condition>lessthan</Condition>
81   <Value1>0.125</Value1>
82   <ThicknessRule id="base">
83     <Condition>greaterthan</Condition>
84     <Value1>0.070</Value1>
85   </ThicknessRule>
86 </FormattingRule>
87 -->
```

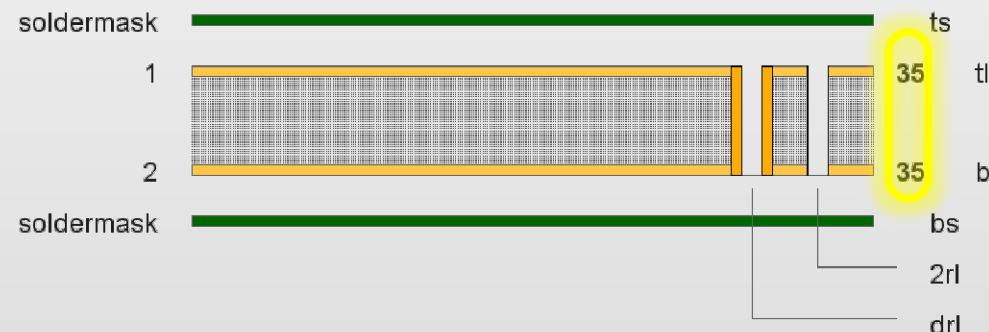
Critical Trace Width	Copper to Copper Clr.
mm	mm
>0.40	<sup>3</sup> 0.23

## QED中的每层成品和基础铜厚度

- 例如，在gbr job文件中包括铜砒码以及其他产品参数，将其添加到归档文件中并提交给Integr8tor

- 简单，轻松，顺畅……

(QED PDF报告补充)



Files - Original					
Initial	Renamed	Function	Position	Color	Thickness
					Base
					Finished

## 登记在工作上花费的互动时间

- 找出您的操作员在“至Ucam”会议期间以互动方式花费多少时间在工作上
- 识别提供需要系统手动干预的数据集的客户，并启动对话以使数据达到标准

*(Cockpit客户端 扩充)*

Original Data	Interactive Time
CDIpinv1.40vp (ID 18941).zip	01:21
107665.zip	00:00
107470.zip	00:00
107154.zip	00:00
107084.zip	
106488.zip	01:17
106046.zip	00:00
105847.zip	00:00
105832.zip	00:00



## 自动注销

- 例如在网络或VPN崩溃后，具有闲置或陈旧的Cockpit会话会自动终止
- 避免用尽Cockpit许可证，因为用户忘记注销

*(Cockpit用户端扩充)*

Auto log-off

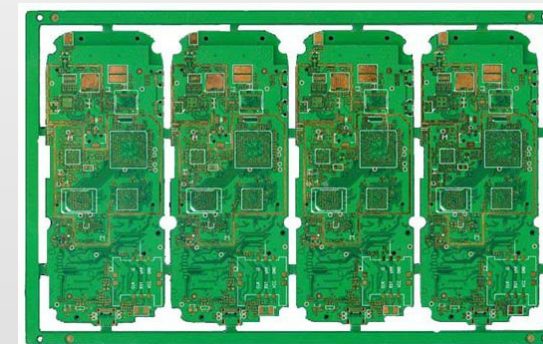
Automatic log-off after

minutes

## 成型长度计算分析

- 组装面板布线对成本和交货时间的影响很大
- 新的QED面板成型长度有助于预测这一情况

(自动分析和QED PDF报告扩充)



Customer Panel (Delivery Array, Shipping Panel) - Original									
Original Image	Panel Size	Left Border	Right Border	Top Border	Bottom Border	X Spacing	Y Spacing	PCB's	Depanel Rout Length
	mm x mm	mm	mm	mm	mm	mm	mm		mm
Single PCB	178.021 x 143.000	15.000	15.000	10.000	10.000	5.000	3.000	3 x 2	1914.126

## 增加新的表面处理和阻焊层颜色

- 附加的阻焊层颜色和表面光洁度可支持您的最新制造  
(除了现有的驾驶舱, 电子邮件输入集成, Web输入集成, Hotfolder输入集成)

## QED阻焊层分析扩展

- 进行精确分析, 以报告通孔顶部和底部的不同阻焊层开口, 以帮助避免生产中的意外情况  
(自动分析和QED PDF报告扩充)

## 带注释的QED PDF

- 我们新样式的QED PDF中的工具提示使新手用户可以立即找到自己的方式……

(QED PDF报告扩充)

Partly Covered Via Holes	One Side Covered Vias ⓘ	Both Sides Covered Vias ⓘ	No Side Covered Vias ⓘ
No			

Through-hole vias that are either (partially) covered by soldermask on the top layer and (partially) free on the bottom layer or (partially) free on the top layer and (partially) covered on the bottom layer.

## QED PDF摘要表修订

- 一站式查找所有电路板必需品的位置已经过优化，为您提供方便和舒适

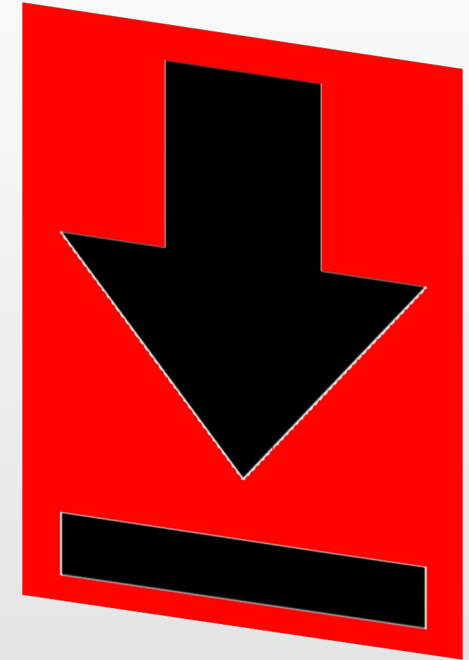
(QED PDF报告扩充)

Summary - General - Original			
PCB Size	95 mm x 103.5 mm	Customer Panel Size	
PCB Thickness	1.6 mm	Max. Aspect Ratio on PTH	8.0
Copper Layers	6	Pressing Stages	1
Surface Finish	unknown	Drill Hole Density	2101 Holes/dm <sup>2</sup>
Solder Mask	Both	Testable Points	1508
Solder Mask Color	unknown	Min. SMD/BGA Size	0.28 mm
Legend	No	Via in Pad	No
Legend Color		Stacked Vias	No
Edge Connector Area	0 dm <sup>2</sup>	Castellated	No
Peeloff Mask	No	Anomalies	No
Carbon Mask	No		

# 安装 v2020.12



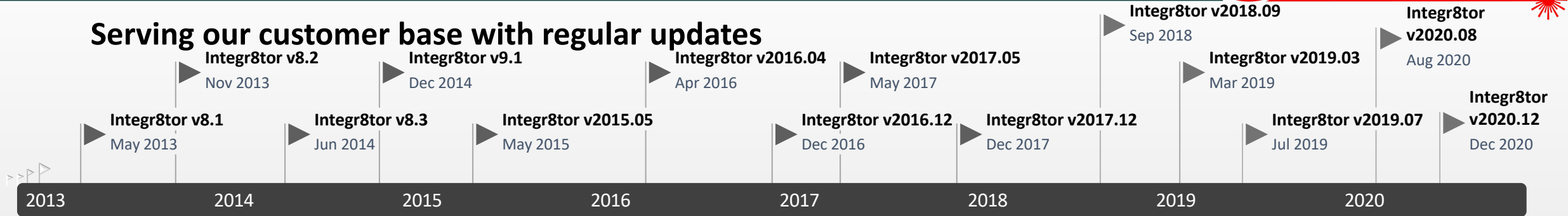
- 下载安装程序  
<ftp://ftp.ucamco.com/Integr8tor>
- 感谢您选择Ucamco产品
- 我们建议您尽早安装此更新。
- 如有其他疑问，请联系我们的当地业务合作伙伴或Ucamco服务台。
- 欢迎关注Ucamco微信公众号（如右图）。



# 提供定期更新服务



## Serving our customer base with regular updates



Version	Release date	Highlights	
8.1	May-13	Support for ODB++ v7.	Compatible with Windows server 2012 and windows 8.
8.2	Nov-13	Detection and flagging of duplicate archives.	Edge connector recognition.
8.3	Jun-14	New standard parameters.	Determination of laser/mechanical drilling.
9.1	Dec-14	Support for Gerber X2 datasets.	Optimized and new QED values.
2015.05	Jun-15	New standard parameters.	Determination of laser/mechanical drilling.
2016.04	Apr-16	SMD/BGA pads differentiates copper- and solder mask defined	DFM Checks (former Capabilities) revised
2016.12	Dec-16	Introducing Integr8tor Job Perspectives	Drill hole tolerances
2017.05	May-17	Support for PCB Surface finish	Same-sized jobs detection
2017.12	Dec-17	Checkpoint review extensions for various QED results	Analysis of via holes with different solder mask openings top/bottom
2018.09	Sep-18	New QED feature: Minimum Critical Trace Width	User-selectable layer registration
2019.03	Mar-19	Measure functionality and freely displayable layers in Checkpoint	Extended import&export support for advanced ODB++ features
2019.07	Jul-19	Introducing C8 Inspect	QED Ring Analysis per tool function
2020.08	Aug-20	UcamX Workflow Edition	Must-have QED and Autoclean Additions
2020.12	Dec-20	QED Backdrill analysis	Altium PCB Input Connector

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